

Characterization and Simulation of High Speed CMOS Operational Amplifier Using Split-length Compensation

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Abstract- An analytical design guide was formulation for the design of 3-stage CMOS Op-Amp with the Split-length Compensation. The proposed design guide generates straight-forwardly the design parameters such as W/L ratio and current of each transistor from the given specification, such as, gain-bandwidth, phase margin, the ratio of compensation capacitance to load capacitance. The OPAMP is designed to exhibit a unity gain frequency of 1.25GHz and exhibits a gain of 79.87dB with an 89.68 phase margin. Design has been carried out in Mentor graphics tools. The results are compared with respect to standard characteristics of the op-amp with the help of graph and table. Simulation results agree with theoretical predictions. Simulations confirm that the settling time can be further improved by increasing the value of GBW; the settling time is achieved 49ns. It has been demonstrated that when W/L increases the parameters GBW increases and settling time reduces so the speed of Op-Amp is high.

Keywords-CMOS analog Circuit, 3-stage CMOS Op-Amp, Stability, GBW, Device design, Frequency Compensation.

I. INTRODUCTION

Over the last few years, the electronics industry has exploded. The largest segment of total worldwide sales is dominated by MOS market. CMOS technology continues to mature with minimum feature sizes now. Designing high performance analog integrated circuits is becoming increasingly exigent with the relentless trend toward reduced supply voltages and transistor channel length. A large part of the success of the MOS transistor is due to the fact that it can be scaled to increasingly smaller dimensions, which results in higher performance. The feature size of individual transistor is shrinking from deep sum-micrometer (DSM) to even nanometer region. As the scale of integration improves, more transistors, faster and smaller than their predecessors, are being packed into a chip. This leads to the steady growth of the operating frequency and processing capacity per chip. Operational Amplifier is the most common building blocks of most of the electronics system may not need introduction. The design of OPAMPs continues to pose a challenge as the supply voltage and transistor channel lengths scale down with each generation of CMOS technologies. At different aspect ratio, there is a tradeoff among speed, power, gain and other performance parameters. The realization of a CMOS OPAMP that combines a considerable dc gain with high unity gain frequency has been a difficult problem. There have been several circuit approaches to evade this problem.

The aim of the design methodology in this paper is to propose straightforward yet accurate equations for the design of high-gain 2 staged CMOS op-amp. To do this, a simple analysis with some meaningful parameters (phase margin, gain-bandwidth, *etc.*) is performed. The method handles a very wide variety of specifications and constraints. In this paper, we formulate the CMOS op-amp design problem and their aspect ratios. The method we present can be applied to a wide variety of amplifier architectures, but in this paper we apply the method to a specific two stage CMOS op-amp.

The variation in the performance of the op-amp with variations in the width and length of the CMOS and the effect of scaling the gate oxide thickness is discussed.

The simulation results have been obtained by TSMC 0.18 micron CMOS technology. Design has been carried out in Mentor Graphics tool. Simulation results are verified using Model SimEldo and Design Architect IC. Scaling effects are analyzed through experimental data and computer simulations. This search technique can be successfully applied to a class of optimization problems. After the simulation, most of the transistors' size still needed to be modified in order to optimize the performance. High gain in operational amplifiers is not the only desired figure of merit for all kind of signal processing applications. Simultaneously optimizing all parameters has become mandatory now a day in operational amplifier design. In this case, the slew rate will increase for an increase in current. However, if the widths of the devices are increased with the bias voltages held constant. Thus, we can conclude that the selection of device sizes depends on trade-offs between stability (phase margin) and slew-rate. As such, for the fastest slew-rate, the smallest channel length (180 nm) will be used, and at this length, the device is in the short channel regime and will require short channel topologies.

II. SPLIT-LENGTH COMPENSATION

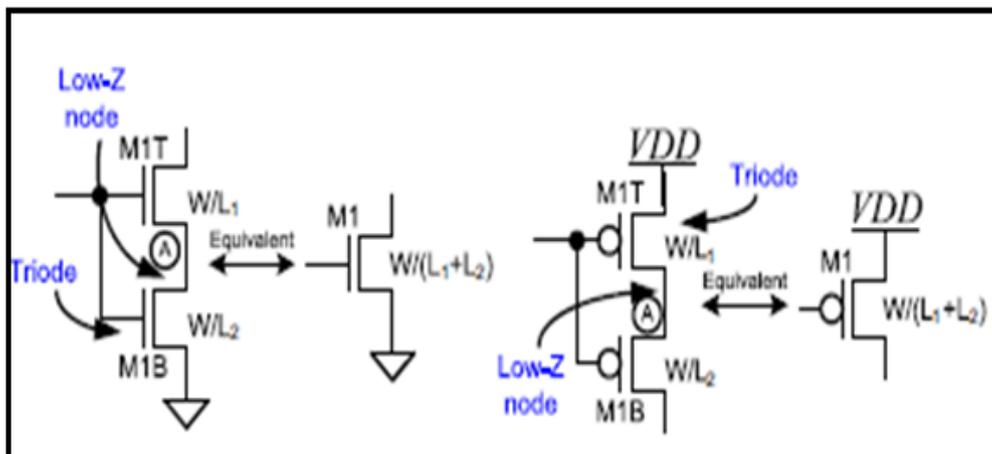


Figure 1. Illustration of the split-length NMOS and PMOS devices and the low impedance nodes^[7]

It is well known that if the compensation current from the output node is fed back to the internal nodes, using a current buffer structure, significant improvement in op amp performance can be achieved. These compensation methods give rise to left-half plane (LHP) zero, instead of a right half plane (RHP) zero (which degrades the phase), and thus enhance the phase margin[6]. In nano-CMOS processes low voltage, high-speed op-amps can be designed by employing a split-length composite transistor for compensation instead of using a common-gate transistor in the cascode stack. Fig.1 illustrates the splitting of an n-channel MOSFET (NMOS) or a p channel MOSFET (PMOS) to create a low impedance internal node-A[7].

In two-stage op-amps employing split-length compensation, pole splitting is achieved with a lower value of the compensation capacitor (C_c) and with a lower value of second-stage transconductance (g_{m2}). This results in a much larger unity gain frequency (ω_{un}) attainable by the op-amp, with lower power consumption and a smaller layout, when compared to the Miller compensated op-amps.

III. SPLIT-LENGTH COMPENSATION OF 3-STAGE OP-AMPS

Continued interest in the three-stage Op-Amp design has seen numerous three-stage Op-Amp design techniques. However, they exhibit either complex implementation or larger power consumption when compared to the commonly used two-stage Op-Amps. This section provides a tutorial on the design techniques, introduced by the author in [8],[9], which result in high-speed and low power three-stage Op-Amps.

A. Three-stage Op-Amp Compensation

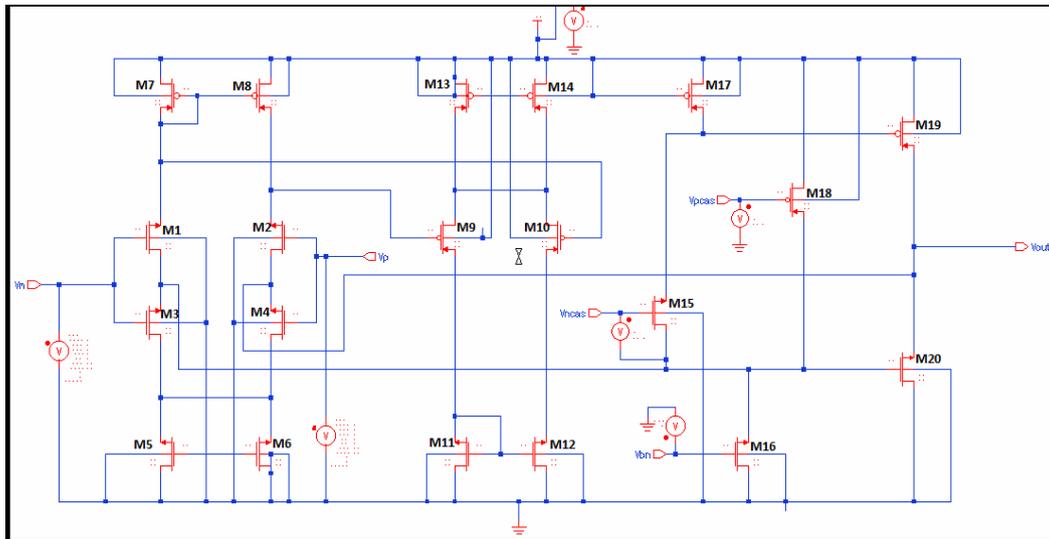


Figure 2. low power, pole zero cancelled class AB, three stage Op-Amp^[8]

The split-length compensation scheme is applied to three-stage op-amp design. A reverse nested compensation topology is used so that the output is not loaded by both of the compensation capacitors, which results in a larger unity gain frequency (ω_{un}). Fig.2 shows a reverse-nested split-length compensated (RSLC), class-AB three-stage op-amp. A stack of maximum three transistors is used to realize the low-VDD gain stages. In this topology an NMOS diff-amp is cascaded with a PMOS diff-amp which is followed by a class-AB output buffer. The PMOS diff-pair in second stage employs wider devices to increase the input common-mode range of the second stage. A split-length diff-pair (SLDP) is used for indirect compensation in order to achieve better supply noise isolation [8]. A diff-amp is employed in the second stage to ensure that the third stage is 'properly' biased by symmetry. The compensation capacitor Cc1 is used to feedback the compensation current ic1 from the output of the second stage (node-2) to the output of the first stage (node-1) through a common gate current buffer. Similarly, capacitor Cc2 is used to feedback current ic2 from node-3 to node-1. Here, the bias voltages $V_{pcas} = V_{DD} - 2V_{SG}$ and $V_{ncas} = 2V_{GS}$ are used to bias the floating current mirror. To ensure overall negative feedback in the circuit, the compensation capacitance must be connected across two nodes which move in opposite direction [8].

B. Small Signal Analysis and Pole-Zero Cancellation

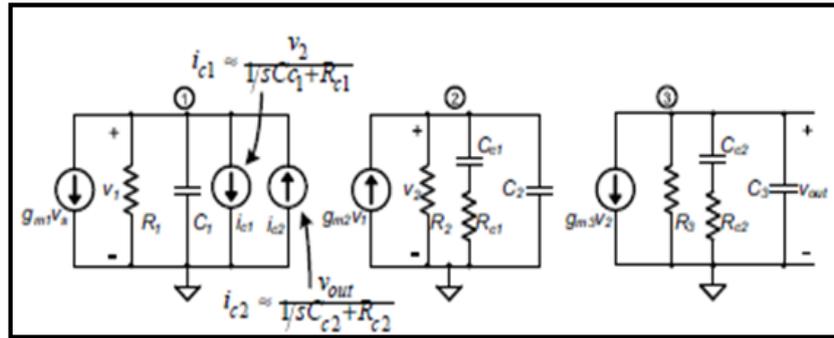


Figure 3. Small Signal Analytical Model for the RSLC Three Stage Op-Amp^[8]

The simplified small signal model for the RSLC three-stage op-amp is shown in Fig. 3 Here, gm1 and gm2 are the transconductances of transistor M2T and M1T respectively. Rc1 and Rc2 are the impedance attached to the nodes fbrand fbl respectively, which are both roughly equal to. Here, gm_k is the transconductance of the kth gain stage while and C_k are the resistance and capacitance respectively, attached to the node-k in the op-amps (k = 1, 2, 3). After applying nodal analysis to the small signal model shown in Fig. 3, the resulting transfer function can be written as [8]

$$H(s) \approx \frac{A_{OL}(1 + b_1s + b_2s^2)}{\left(1 + \frac{a_0}{a_1}s\right)\left(1 + \frac{a_2}{a_1}s + \frac{a_3}{a_1}s^2\right)\left(1 + \frac{a_4}{a_3}s + \frac{a_5}{a_3}s^2\right)} \quad (1)$$

The DC gain AOL is equal to and the unity gain frequency is given as

$$\omega_{\mu m} = \frac{g_{m1}}{g_{m2}} \quad (2)$$

and the dominant pole is located at

$$\omega_{p1} \approx \frac{1}{g_{m3}R_3g_{m2}R_2R_1C_{c2}} \quad (3)$$

The pole-zero cancellation leads to the following design Criterion

$$R_{c1} \approx \frac{C_L}{g_{m3}C_{c2}}, R_{c2} \approx \frac{C_{c1}(C_L + C_{c2})}{g_{m3}C_{c2}^2} \approx \frac{C_{c1}}{C_{c2}}R_{c1} \quad (4)$$

Note that the design equations are independent of the parasitic nodal resistance and capacitance values. The pole-zero cancellation leads to real pole-zero doublets located at [15] (see Fig.4)

$$\omega_{p2} = \omega_{z1} \approx \frac{1}{R_{c1}C_{c1}} = \frac{g_{m3}C_{c2}}{C_{c1}C_L} \quad (5)$$

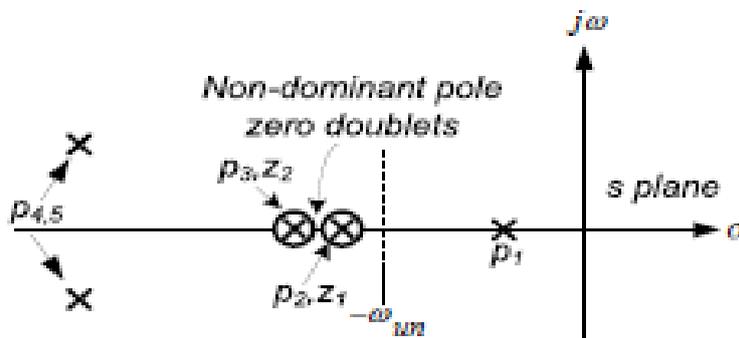


Figure 4. Pole-Zero plot for a typical Spli-length Compensated Three Stage Op-Amp^[8]

$$\omega_{p3} = \omega_{z2} \approx \frac{1}{R_{c2}C_{c2}} = \frac{g_{m3}C_{c2}}{C_{c1}(C_L + C_{c2})} = \frac{\omega_{p2}}{1 + \frac{C_{c2}}{C_L}} \quad (6)$$

From above two Eq. , we can see that the non-dominant pole-zero doublets appear close together in the frequency domain. The pole-zero doublets should be placed at a frequency higher than the ω_{un} of the op-amp, which results in the upper bound on ω_{un} [8].

$$\omega_{\mu n} \leq \sqrt{\frac{g_{m1}g_{m3}}{C_{c1}C_L}} \tag{7}$$

The location and quality factor of the parasitic conjugate poles due to the loading of nodes fbl and fbr are given by

$$(\omega_{p4,5}) \approx \frac{g_{m3}C_{c2}}{C_L} \sqrt{\frac{g_{m2}R_2C_{c2}}{C_1C_2C_{c1}}} \tag{8}$$

$$Q_{4,5} \approx \sqrt{\frac{g_{m2}R_2}{R_{c1}R_{c2}}} \left(\frac{1}{\frac{1}{R_1} \sqrt{\frac{C_1}{C_2}} + \frac{1}{R_2} \sqrt{\frac{C_2}{C_1}}} \right) \tag{9}$$

The mirror poles in the diff-amps are located at a higher frequency than the poles ω_{p1-5} . The phase margin for the opamp can be approximated as

$$\phi_M \approx 90^\circ - \tan^{-1} \left(\frac{\frac{\omega_{\mu n}}{Q_{4,5}}}{1 - \left(\frac{\omega_{\mu n}}{\omega_{4,5}}\right)^2} \right) \tag{10}$$

It can be observed that the location of the parasitic poles and hence the phase margin is dependent upon the choice of open loop gain in the second stage. The slew-rate for these opamps can be estimated as $\min\left(\frac{I_{ss1}}{C_{c1}}, \frac{I_{ss2}}{C_{c2}}\right)$, where I_{ssk} are the diffamp tail currents. A detailed comparison of the RSLC opamps with the prior literature is provided in.

IV. DESIGN PARAMETERS AND SIMULATION RESULTS

Table I- The Design Parameter

M1,M2,M3,M4	W/L=50um/0.18um
M5,M6,M11,M12,M15,M16	W/L=10um/0.18um
M9,M10	W/L=66um/0.18um
M7,M8,M13,M14,M17,M18	W/L=22um/0.18um
M19	W/L=110um/0.18um
M20	W/L=40um/0.18um
C_{c1}	3pf
C_{c2}	1.5pf
R_{c1}	9.5K
R_{c2}	1.18K

A. Transient Analysis in 180nm Technology

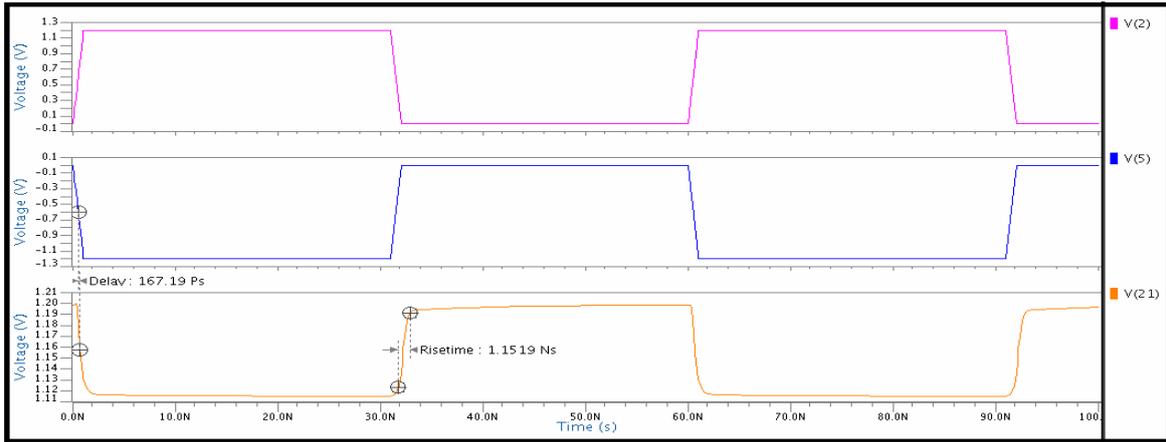


Figure 5. Transient Analysis in 180 nm technology

B. Ac Response in 180nm Technology

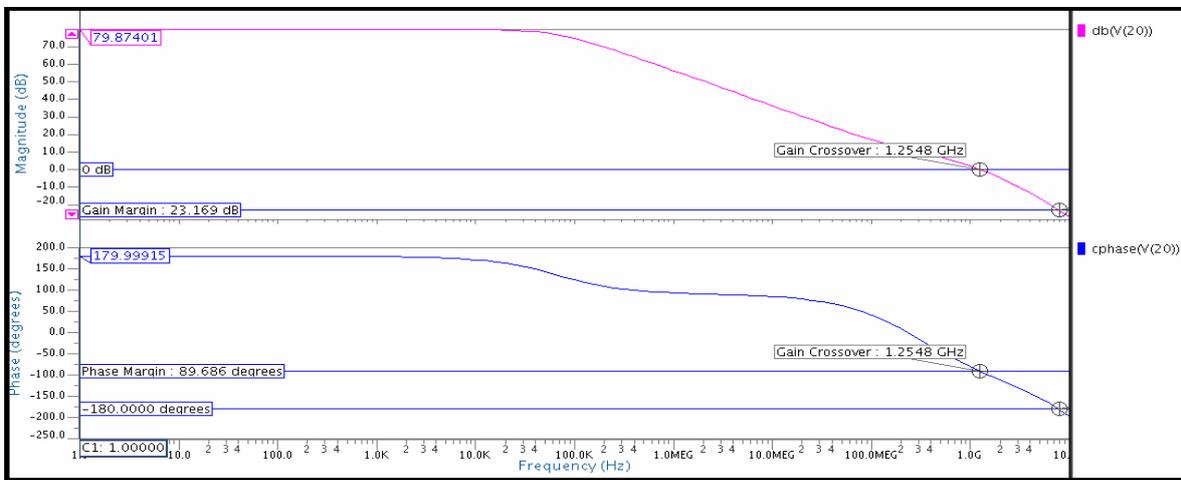


Figure 6. AC Response in 180 nm technology

C. Slew rate in 180nm Technology

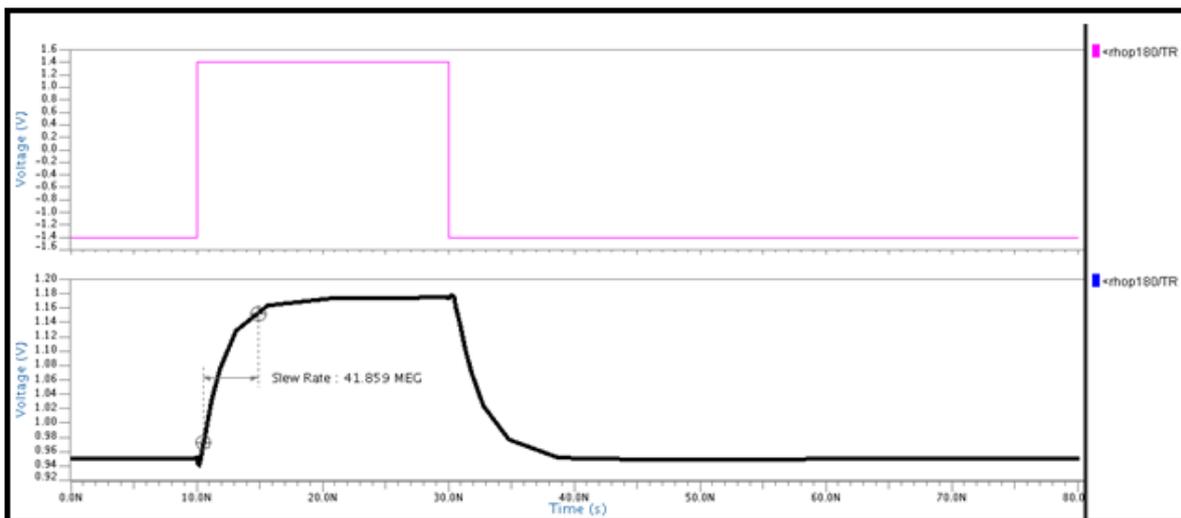


Figure 7. Slew rate in 180 nm technology

D. Offset Analysis in 180nm Technology

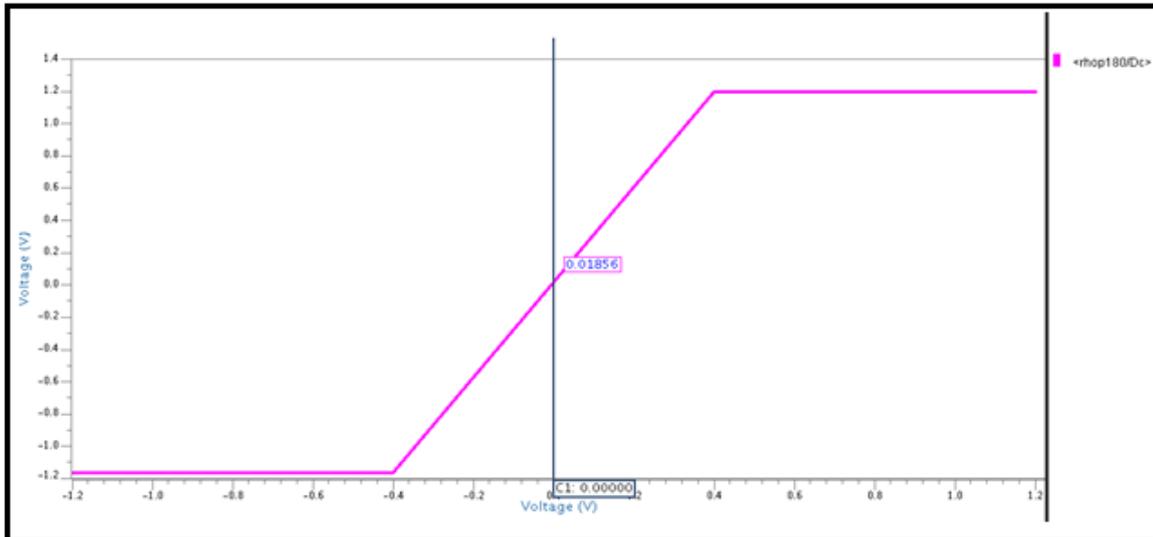


Figure 8. Offset Analysis in 180 nm technology

V. TABLE

Parameters	Technology
	180nm
Supply Voltage	1.2V
Gain	79.87dB
Phase Margin	89.68 degree
Delay	167.19ps
Offset	0.02V
Slew rate	41.86MHz

VI. CONCLUSION

A methodology has been presented to design split-length compensated three-stage Op-Amp suitable for low-voltage nano-CMOS technology. A toolkit has been created and made available to simplify the compensation procedure for three-stage Op-Amps and for understanding the dynamics of multi-pole and zero Op-Amp systems. A 0.18 μ m CMOS process with 1.2V supply voltage was used in the design. Here, we get the 79.87dB gain and 167.19ps delay in 180nm technology.

VII. REFERENCES

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